REMARKS

Claims 1-4 are amended. Claims 7 and 8 are new. No new subject matter is added. Reconsideration and allowance of claims 1-8 is requested in light of the following remarks.

Claim Rejections – 35 U.S.C. § 103

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,424,011 to Assaderaghi, et al. ("Assaderaghi") in view of U.S. Patent No. 5,767,549 to Chen, et al. ("Chen"). The applicant disagrees.

Claim 1 is amended to improve the clarity of the claim and to remove any implication, valid or not, that the claim is a product-by-process claim. Thus, where appropriate, the word "formed" has been replaced with "disposed."

Claim 1 is amended to recite, *inter alia*, a SOI layer disposed on an upper surface of the BOX layer, the SOI layer including an active area and a device isolation area, the device isolation area including a well that is doped with impurities. The above features are fully supported by the original application at, e.g., FIG. 3B; FIG. 4A; page 7, lines 6-7; and original claim 1. In particular, the features of an SOI layer having an active area and a device isolation area can be found in original claim 1, at lines 3 and 6. The feature of a well formed in a device isolation area of the SOI layer can be found in original claim 1, at line 3.

It is alleged that the SOI islands shown by Assaderaghi (FIG. 5e) are wells. However, Assaderaghi also shows that the so-called SOI islands are formed in areas of the SOI layers that include the source regions and drain regions. See, e.g., FIGs. 2a, 2b and 2c. It is well known that source and drain regions are found in the active areas of a device.

To the contrary, claim 1 recites that the SOI layer includes an active area and a device isolation area, and that the device isolation area includes a well. Assaderaghi contains no teaching that a device isolation area of the SOI layer includes a well. See, e.g., FIGs. 2a, 2b and 2c. Furthermore, Chen contains no teaching that a device isolation area of the SOI layer includes a well.

Consequently, the Assaderaghi/Chen combination fails to establish a *prima facie* case of obviousness for claim 1 because it does not teach or suggest all the features in the claim. MPEP 2143.03.

Furthermore, it was alleged that Assaderaghi shows a field oxide film (202) formed adjacent to the well (figure 5a), and then admitted that Assaderaghi fails to show the recited feature of a field oxide film disposed on an upper surface of the well.

The applicant notes that the Assaderaghi actually refers to the 202 regions as shallow isolation regions (column 9, lines 65-67). Thus, the shallow isolation regions 202 more properly correspond to the recited device isolation area of the SOI layer. As was noted above, Assaderaghi's shallow isolation regions 202 do not have wells.

Chen teaches that field oxide layer 28 may be grown on a surface of a silicon layer 18 in a recessed region 20 (FIG. 1; column 3, lines 21-25), and the Examiner is apparently motivated to combine this teaching with Assaderaghi so that the bottom of the well (silicon layer 18) is in contact with the BOX layer 14. However, as shown in FIG. 5a, the bottom of Assaderaghi's alleged wells (SOI islands) are already in contact with the BOX layer.

Thus, there is no suggestion or motivation to modify Assaderaghi with Chen in the manner that is suggested.

For this additional reason, the Assaderaghi/Chen combination fails to establish a *prima facie* case of obviousness for claim 1. MPEP 2143.01.

Claims 2-3 depend from claim 1. Consequently, claims 2-3 are allowable over the Assaderaghi/Chen combination because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Claim 4 is amended to improve the clarity of the claim and to remove any implication, valid or not, that the claim is a product-by-process claim. Thus, where appropriate, the word "formed" has been replaced with "disposed."

Claim 4 recites, *inter alia*, that the first and second active areas are adjacent to the well.

It is alleged that the SOI islands shown by Assaderaghi (FIG. 5e) are wells. However, Asserderaghi teaches that a source region 20 and drain region 22 are provided in a SOI layer of a SOI substrate 24, with shallow trench isolation regions 26 and 28 provided in the SOI substrate adjacent to the source and drain regions (FIG. 2a; column 5, lines 48-52). The SOI islands illustrated in FIG. 5e clearly have the same source/drain structure as shown in FIGs. 2a, 2b and 2c, and they are located beneath transistor gates. Since it is well known that source and drain regions are found in the active areas of a device, the alleged wells (SOI islands) must also be in active areas of the device. If the alleged wells located in active areas of the device, then, contrary to claim 4, the alleged wells cannot be adjacent to active areas of the device.

Chen also fails to show first and second active areas adjacent to the alleged well (FIG. 1; silicon layer 18).

For the above reason, the Assaderaghi/Chen combination fails to establish *prima facie* obviousness for claim 4 because it does not teach or suggest all the features recited in the claim. MPEP 2143.03.

Furthermore, claim 4 recites that the insulation layer is in contact with a sidewall of the gate line. This feature is fully supported by the original application at, e.g., FIG. 3B and original claim 4, which recited "the insulation layer covering a lower portion of the gate line."

It is alleged that the recited gate line is disclosed by the n-gate of Assaderaghi FIGs. 7b and 8b. However, FIG. 7b shows that the sidewalls of the alleged n-gate are completely covered by a layer that has no reference numeral. This un-referenced layer is not the same as the layers 211, 217 that were previously alleged to the recited insulating layer. In fact, the un-referenced layer that covers the sidewalls of the n-gate cannot be the recited insulation layer because, contrary to claim 4, it is not disposed on the alleged field oxide film (202). Chen also fails to disclose this feature.

For this additional reason, the Assaderaghi/Chen combination fails to establish *prima facie* obviousness for claim 4. MPEP 2143.03.

Claims 5-6 depend from claim 4. Consequently, claims 2-3 are allowable over the Assaderaghi/Chen combination because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Claims 1-6 are alternately rejected under 35 U.S.C. 103(a) as being unpatentable over Assaderaghi in view of Chen and U.S. Patent No. 6,426,558 to Chapple-Sokol, et al. ("Chappel-Sokol"). The applicant disagrees.

The failure of Assaderaghi and Chen to teach or suggest all features of claims 1 and 4, as described above, are not remedied by Chappel-Sokol. Furthermore, the use of Chappel-Sokol is based upon the alternate assumption that the recitation of an opening and an LIC implies certain method steps that affect the final structure. As noted above, claims 1 and 4 are amended to remove any implication, valid or not, that the claims 1 and 4 are product-by-process claims.

New Claims 7-8

New independent claim 7 is added. No new subject matter is added, as all recited claim features are supported by the original application, at, e.g., claim 1, claim 4, and FIG. 3B. New dependent claim 8 is supported by the original application at, e.g., claims 2 and 3.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-8 is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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